CLAIMS

What is claimed is:

1. A method for generating an integrated circuit layout, comprising the steps of:

receiving an integrated circuit netlist describing a plurality of transistors and a plurality of conductors for interconnecting the plurality of transistors, each of the plurality of transistors having a width in a layout corresponding to the integrated circuit netlist;

determining that more than one of the plurality of transistors are the widest transistors and that the more than one widest transistors all have the same width;

folding only one of the widest transistors to produce a folded transistor that is electrically equivalent to the widest transistor, the folded transistor having at least two fingers, each finger having a smaller width than the width of the widest transistors; and

creating a fold solution for the layout with the one folded transistor.

2. The method of claim 1, wherein the steps of folding and creating are repeated for each of the plurality of transistors until all of the plurality of transistors have been folded at least once.

3. The method of claim 2, wherein the plurality of transistors includes a plurality of N-channel transistors and a plurality of P-channel transistors and the steps of folding and creating are repeated for each transistor of the plurality of N-channel transistors to create an independent N-channel fold solution list and the steps of folding and creating are repeated for each transistor of the plurality of P-channel transistors to create an independent P-channel fold solution list.

4. The method of claim 3 further comprising the steps of:

receiving a dependency map for listing dependent pairs of N-channel and P-channel transistors from the integrated circuit netlist;

summing the widths of the dependent pairs to generate a height lower bound;

folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list; and

merging the independent N-channel fold solution list, the independent P-channel fold solution list, the N-channel

dependent fold list and the P-channel dependent fold list to produce an initial fold solution list.

5. The method of claim 4, further comprising the step of selecting a fold solution from the initial fold solution list.

6. The method of claim 5 further comprising the step of create modified fold solution from the selected fold solution based on predetermined cell layout information.

7. The method of claim 6 further comprising the steps of:

placing transistors from the modified fold solution list in the integrated circuit layout;

defining a routing channel between the plurality of P-channel transistors and the plurality of N-channel transistors;

calculating a predetermined metric for the modified fold solution; and

generating the integrated circuit layout.

8. The method of claim 7, wherein the method is implemented as software on a data processing system.

9. A method for generating an integrated circuit layout comprising the steps of:

receiving an integrated circuit netlist describing a plurality of P-channel transistors, a plurality of N-channel transistors, and a plurality of conductors for interconnecting the plurality of N-channel transistors and the plurality of P-channel transistors, each of the transistors having a width in a layout corresponding to the integrated circuit netlist;

folding the widest transistors of the plurality of N-channel transistors and the plurality of P-channel transistors to produce a list of folded N-channel transistors and a list of folded P-channel transistors, each folded transistor having at least two fingers, each finger having a smaller width than the width of its corresponding unfolded transistor, and each folded transistor being electrically equivalent to its corresponding unfolded transistor;

receiving a dependency map for listing dependent pairs of N-channel and P-channel transistors from the integrated circuit netlist;

summing the widths of the dependent pairs to generate a height lower bound;

folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list; and

merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list.

10. The method of claim 9, wherein a fold solution from the initial fold solution list is selected based on a predetermined selection criteria.

11. The method of claim 10 further comprising the step of creating a modified fold solution from the selected fold solution based on predetermined cell layout information.

12. The method of claim 11 further comprising the steps of:

placing transistors from the modified fold solution in the integrated circuit layout;

defining a routing channel between the plurality of P-channel transistors and the plurality of N-channel transistors;

calculating a predetermined metric for the modified fold solution; and

generating the integrated circuit layout.

13. The method of claim 12, wherein the method is implemented as software on a data processing system.

14. A method for generating an integrated circuit layout comprising the steps of:

receiving a base logical cell structure describing a plurality of transistors and a plurality of conductors for interconnecting the plurality of transistors, each of the transistors having a width in a layout corresponding to the base logical cell structure;

iteratively folding only one transistor at a time of the plurality of transistors that have a width greater than a predetermined width to produce two transistors, each of the two transistors having a width shorter than the width of a corresponding unfolded transistor; and

after each iteration, creating a fold solution after each iteration and adding the fold solution to a fold solution list.

15. The method of claim 15, wherein the base logical cell structure is a portion of an integrated circuit netlist for defining an integrated circuit.

16. The method of claim 15, further comprising the steps of:

receiving the integrated circuit netlist describing a plurality of transistors and a plurality of conductors for interconnecting the plurality of transistors, each of the plurality of transistors

having a width in a layout corresponding to the integrated circuit netlist;

determining that more than one of the plurality of transistors are the widest transistors and that the more than one widest transistors all have the same width;

folding only one of the widest transistors to produce a folded transistor that is electrically equivalent to the widest transistor, the folded transistor having at least two fingers, each finger having a smaller width than the width of the widest transistors; and

creating a fold solution for the layout with the one folded transistor.

17. The method of claim 16, wherein the steps of folding and creating are repeated for each of the plurality of transistors until all of the plurality of transistors have been folded at least once.

18. The method of claim 17, wherein the plurality of transistors includes a plurality of N-channel transistors and a plurality of P-channel transistors and the steps of folding and creating are repeated for each transistor of the plurality of N-channel transistors to create an independent N-channel fold solution list and the steps of folding and creating are repeated for each transistor of the plurality of P-channel transistors to create an independent P-channel fold solution list.

19. The method of claim 18 further comprising the steps of:

receiving a dependency map for listing dependent pairs of N-channel and P-channel transistors from the integrated circuit netlist;

summing the widths of the dependent pairs to generate a height lower bound;

folding transistors of the dependent pairs having a height lower bound greater than a predetermined amount to produce an N-channel dependent fold list and a P-channel dependent fold list; and

merging the independent N-channel fold solution list, the independent P-channel fold solution list, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list.

20. The method of claim 19, further comprising the step of selecting a fold solution from the initial fold solution list.

21. The method of claim 20, further comprising the step of creating a modified fold solution from the selected fold solution based on predetermined cell layout information.

22. The method of claim 21, further comprising the steps of:

placing transistors from the modified fold solution list in the integrated circuit layout;

defining a routing channel between the plurality of P-channel transistors and the plurality of N-channel transistors;

calculating a predetermined metric for the modified fold solution; and

generating the integrated circuit layout.

23. A method for generating an integrated circuit layout comprising the steps of:

receiving a base logical cell structure describing a plurality of P-channel transistors, a plurality of N-channel transistors, and a plurality of conductors for interconnecting the plurality of N-channel transistors and the plurality of P-channel transistors, each of the transistors having a width in a layout corresponding to the base logical cell structure;

receiving a dependency map for listing dependent pairs of N-channel and P-channel transistors from the base logical cell structure; and

folding transistors of the plurality of N-channel transistors and the plurality of P-channel transistors based on a predetermined parameter of the dependency map, wherein the step of folding a transistor produces two transistors, each of the two

transistors having a width shorter than the width of a corresponding unfolded transistor.

24. The method of claim 23, wherein the predetermined parameter of the dependency map is a height lower bound determined by summing transistor widths of each of the dependent pairs.

25. The method of claim 23, further comprising the step of:

folding the widest transistors of the plurality of N-channel transistors and the plurality of P-channel transistors to produce a list of folded N-channel transistors and a list of folded P-channel transistors, wherein the list of folded N-channel transistors and the list of folded P-channel transistors are produced independent of the dependency map.

26. The method of claim 25, wherein the plurality of N-channel transistors and the plurality of P-channel transistors are iteratively folded to an N-channel dependent fold list and a P-channel dependent fold list.

27. The method of claim 26, further comprising the step of merging the list of folded N-channel transistors, the list of folded P-channel transistors, the N-channel dependent fold list and the P-channel dependent fold list to produce an initial fold solution list.

28. The method of claim 27, further comprising the step of selecting a fold solution from the initial fold solution list.

29. The method of claim 28 further comprising the step of create modified fold solution from the selected fold solution based on predetermined cell layout information.